

ABSTRACT OF THE DISCLOSURE

A CAM circuit according to the present invention used for a cash memory and the like, wherein an address is obtained by designating a data, comprises a data compare unit for
5 comparing a data stored in a memory unit to a data of a compare line in a state where a match line is activated and a consistency cancel circuit for forcibly making the match line inactive when a word line and a write instruction signal are both activated. When a write operation and a retrieve operation are
10 simultaneously instructed, a result of the retrieval is forcibly judged to be inconsistent at a write address, thereby it is unnecessary to prohibit the simultaneous execution of the write operation and the retrieve operation.

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